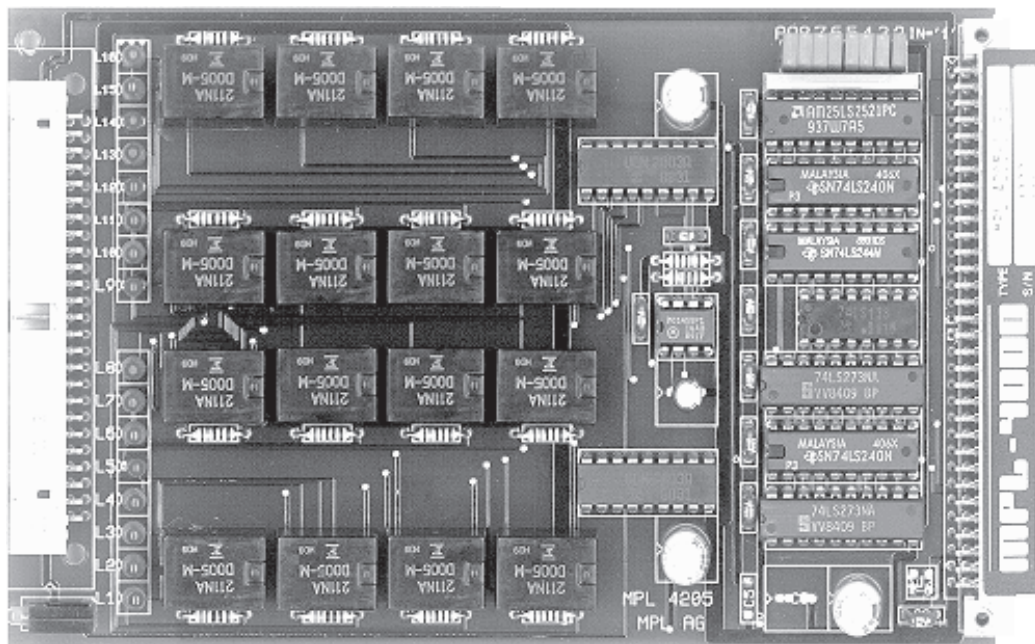


**G-64/96 EUROCARD WITH SIXTEEN RELAYS**

The MPL 4205 provides a simple way to switch external signals via relays. In many applications the user has to connect potential free signals or to switch signals which have not the same ground as the system. The MPL 4205 is the ideal solution in such cases. The card features LED's to indicate the state of the relays.

**TECHNICAL FEATURES:**

- Eurocard format (100 x 160 mm)
- G-64/96 compatible bus
- Parallel output with 16 relays
- All relays with two-way contacts (1 x u)
- All contacts available at the connector
- Breaking capacity: 0.5 A / 100 VAC  
1.0 A / 24 VDC
- Contact-resistance : 100 mOhm (at 6V/0.1A)
- Response-time (on and off) : typ. 5 msec
- Mechanical lifetime : min. 5'000'000 cycles
- Electrical lifetime : min. 100'000 cycles  
(at 0.5A/1000 VAC)  
min. 300'000 cycles  
(at 1.0A/24 VDC)
- LED's to indicate state of the relays



**References**

MPL 4205-1 G-64/96 card with sixteen relays

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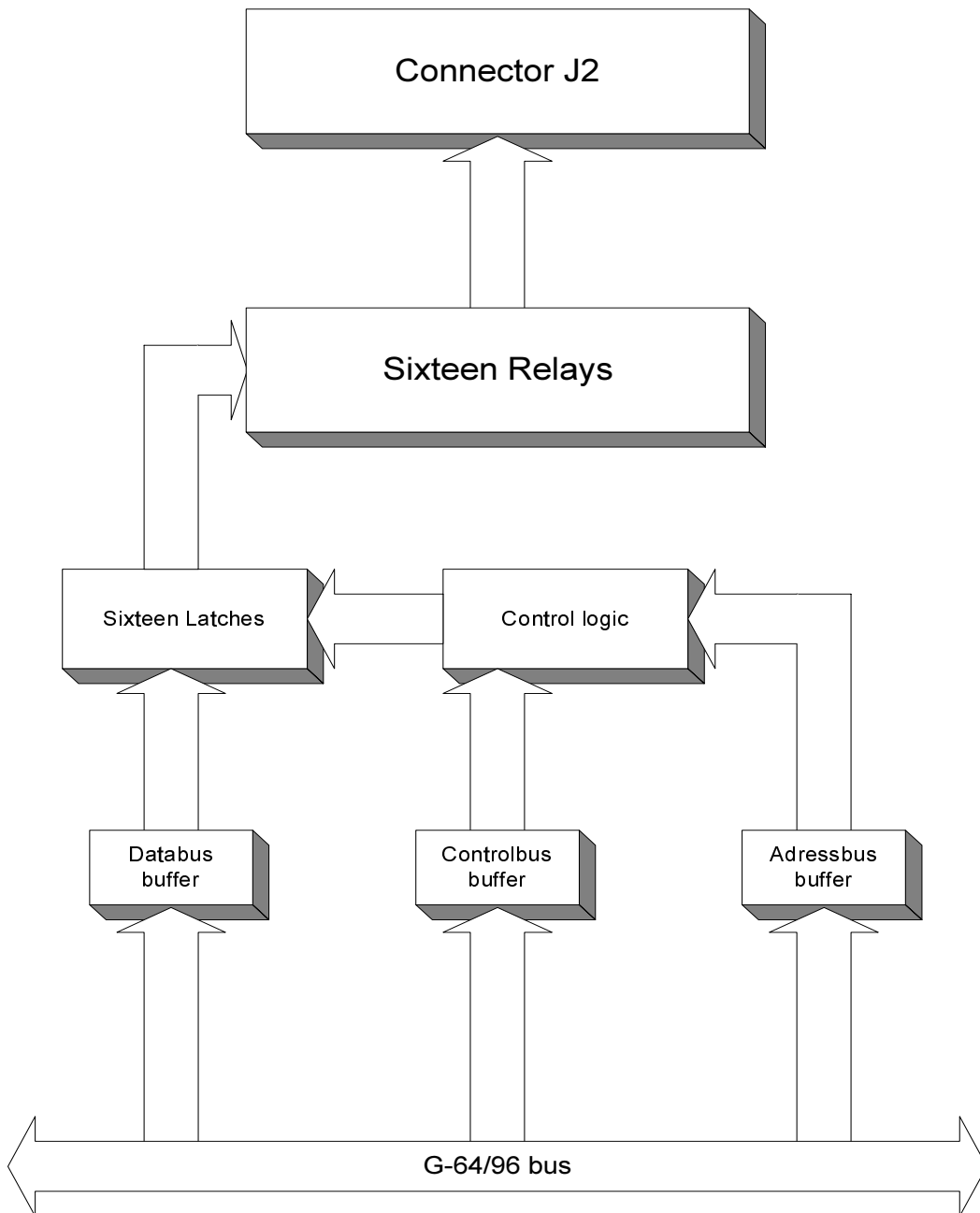


Fig 1. Block diagram

## 1. GENERAL INFORMATION

### 1.1 FUNCTIONAL DESCRIPTION

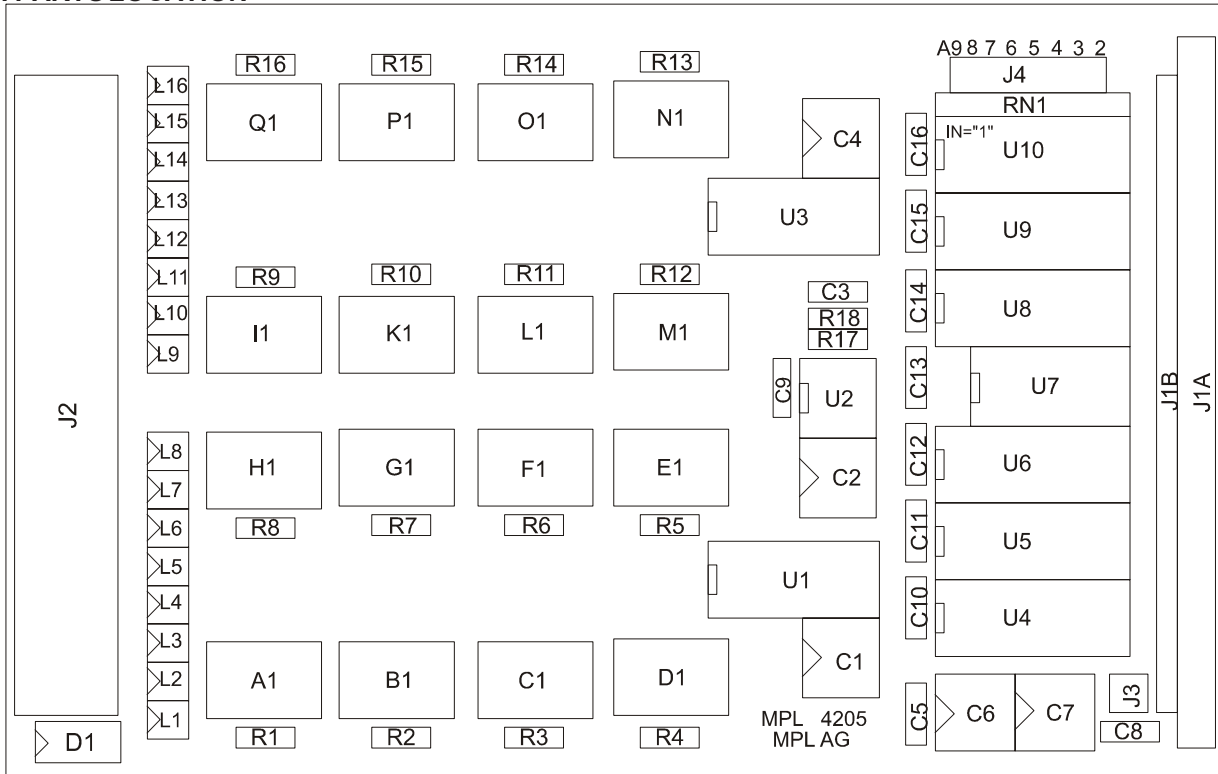
The MPL 4205 provides a simple way to switch external signals via relays. In many applications the user has to connect potential free signals or switch signals which don't have the same ground as the system. The MPL 4205 is the ideal solution in such cases. The card features LED's to indicate the state of the relays.

### 1.2 TECHNICAL CHARACTERISTICS

- Eurocard format (100 x 160 mm)
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- Parallel output with 16 relays
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- Response-time (on and off) : typ. 5 msec
- Mechanical lifetime : min. 5'000'000 cycles
- Electrical lifetime : min. 100'000 cycles (at 0.5A/1000 VAC)  
min. 300'000 cycles (at 1.0A/24 VDC)
- LED's to indicate state of the relays
- Power requirements : +5V 1.5A typ. (all relays on)
- Temperature range : +10 to +50 deg. C, rel. humidity 20-90 % non condensing

## 2. INSTALLATION

### 2.1 PARTS LOCATION



**Fig. 2.1 : Parts location**

## 2.2 JUMPER AND CONNECTOR ASSIGNMENT

J1	G-64/96 connector
J2	Relay contact connector
J3	Internal use
J4	Address selection

Table 2.1

## 2.3 JUMPER CONFIGURATION

Different modes of operation and configuration can be set by means of various jumpers. Their functions are described below:

### 2.3.1 ADDRESS SETTING (J9)

The address at which the card operates is defined by two factors:

- The predecoded base address defined by the CPU-card (VPA)
- An offset defined by the setting of A9-A2

Assuming that the VPA is true from \$EC00-\$EFFF and the MPL 4205 should be at \$EF80, the following jumpers have to be installed:

	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
VPA	1	1	1	0	1	1	X	X	X	X	X	X	X	X	X	X
Offset							1	1	1	0	0	0	0	0	X	X
Address of the card	1	1	1	0	1	1	1	1	1	0	0	0	0	0	X	X
		E				F				8				0		

Table 2.2

The base address of the card (\$EF80) is defined by installing the jumpers A9, A8 and A7. A1 and A0 are undefined since these bits define the card-internal offset.

The card occupies 4 Bytes, so the next card could be addressed at \$EF84!

The offset can be set directly in the jumperfield A9-A2. Each installed jumper represents a "1".

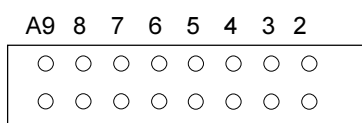


Fig. 2.2 : Card base address jumper (J9)

## 2.4 CONNECTOR PIN ASSIGNMENT

The assignment of the various connectors can be seen from the following tables:

### 2.4.1 G-64 BUS CONNECTOR

The following table gives an overview of the used bus signals and their type.

PIN Nr.	ROWB G-64	used	T	ROWA G-64	used	T
1	GND	•		GND	•	
2	A8	•	TS	A0	•	TS
3	A9		TS	A1	•	TS
4	A10		TS	A2	•	TS
5	A11		TS	A3	•	TS
6	A12		TS	A4	•	TS
7	A13		TS	A5	•	TS
8	A14		TS	A6	•	TS
9	A15		TS	A7	•	TS
10	/BRQ*		OC	BGRT		TS
11	/RRQ*		OC	RGRT		TS
12	/BGACK*		OC	HALT*		OC
13	E	•	TS	MCLK		TS
14	/RES*	•	OC	VPA*	•	TS
15	NMI*	•	OC	RDY		OC
16	IRQ*	•	OC	VMA*		TS
17	FIRQ*	•	OC	R/W*	•	TS
18	IACK		TS	HALTACK		T
19	D12*		TS	D8*		TS
20	D13*		TS	D9*		TS
21	D14*		TS	D10*		TS
22	D15*		TS	D11*		TS
23	D4*	•	TS	D0*	•	TS
24	D5*	•	TS	D1*	•	TS
25	D6*	•	TS	D2*	•	TS
26	D7*	•	TS	D3*	•	TS
27	PERR*		OC	PAGE*		TS
28	CHAININ		T	CHAINOUT		T
29	+5VBATT			-5V		
30	-12V			+12V	•	
31	+5V			+5V	•	
32	GND			GND	•	

Table 2.4.1: G-64 Bus connector

**Note:**

The column T designates the type of the line.

T = TTL

OC = Open collector

TS = Tristate

\* = Inverted signal

• = used

### 2.4.2 LED ASSIGNMENTS

Fig. 2.4.2 shows the relation between relay and the corresponding LED indicator. An illuminated LED means that the corresponding relay is in "NO" (activated) position.

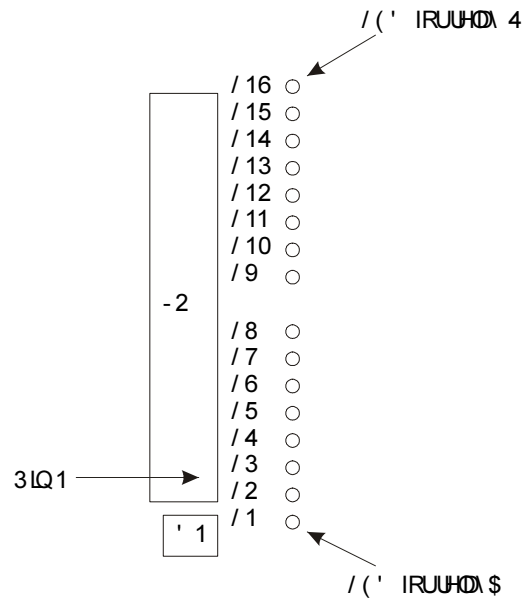















































Fig. 2.4.2 Led assignments

### 2.4.3 I/O CONNECTOR

All contacts of the relays are available via connector J2. The following list shows the pin-assignment.

Pin	Relay
1	 NC
2	 A
3	 NO
4	 B
5	
6	 C
7	
8	 D
9	
10	 E
11	
12	 F
13	
14	 G
15	
16	 H
17	
18	 I
19	
20	 K
21	
22	 L
23	
24	 M
25	
26	 N
27	
28	 O
29	
30	 P
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


Pin	Relay
46	
47	 Q
48	
49	Relay Supply
50	System GND

Table 2.4.3 : I/O connector J2

**Note:**

NC : Normally closed (inactive position)  
 NO : Normally open

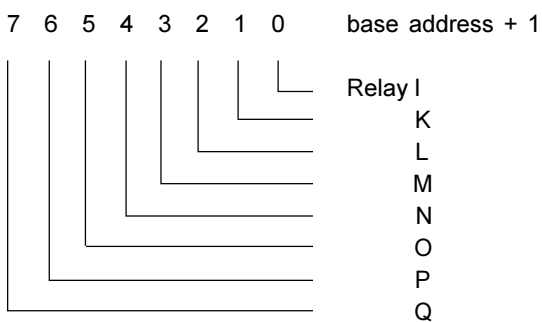
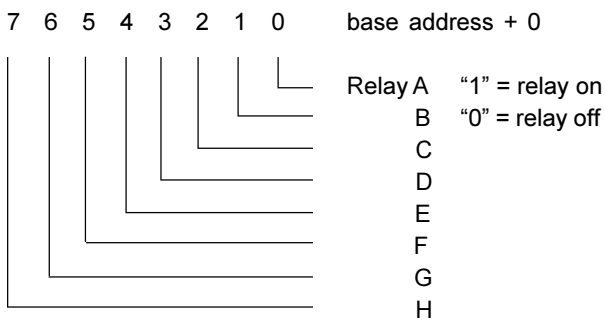
### 3. OPERATION

#### 3.1 THEORY OF OPERATION

The MPL 4205 is very easy to program. It consists of two registers, each representing 8 relays. If the bit in the register is set, the relay is activated. The corresponding LED shows the state of the relay.

#### 3.2 REGISTER ASSIGNMENT

The MPL 4205 has two registers. The register at base-address +0 represents relays A to H; the register +1 the relays I to Q.



#### 3.3 SOFTWARE CONSIDERATIONS

The registers as described in the above paragraph are write-only registers and can not be read back. Bit manipulations must therefore be done in memory and the result must then be written into the corresponding register.

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This manual reflects the Rev.A of the MPL 4205

Publication Date : August 1991

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